CLAIM AMENDMENTS

Listing of Claims:

1. (original) A method for performing deep packet processing on an input variable word bit chain, said method comprising the steps of:

- creating a state table based on at least one initial state, and a final state, each state table entry defining a state-transition rule comprising a s-bit current state, a n-bit word of the input variable word bit chain and as-bit next state;

- converting the entries of the state table into a reduced number of state-transition rule entries, each entry containing a ternary match condition expressed as a s+n-bit test value and a s+n-bit test mask to be applied to the current state and the input word in combination, said each entry further containing the s-bit next state;

- ordering the reduced state table entries obtained by the execution of the preceding step, in a prioritized order, with most frequently used state-transition rules having the highest priority;

-initializing a current state as being the initial state and the first word of the chain being a current input word;

- testing the current state and the current input in combination, against the test value, using the test mask, in all the entries of the reduced state table until a match is found on at least one entry;

- if multiple entries match, selecting one entry with the highest priority;

- if the next state read in the state-transition rule of the selected matching entry is not a final state, defining the next word of the input word chain as being the current input and the next state being the current state; and,

- repeating the testing, selecting and defining steps until a final state is found.

2. (original) The method of claim 1 further comprising, before the initializing step, the steps of:

- defining as a hash index for the reduced state table, a set of i bit locations inside the s-bit current state and the input n-bit word in combination, and an integer N, such that, at most, N table entries can match a hash index value;

- creating a compressed state table, indexed by the hash index, having 2^i entries, each entry corresponding to one value of the hash index, and each having a maximum of N state-transition rules of the reduced state table
corresponding to the same hash index value and written in a priority order;

- saving an s + n bit index mask corresponding to the hash index, and saving a base address pointer of the compressed state table;

said method being also characterized in that the testing step further comprises an initial step of identifying the hash index of the current sate and current input in combination, using the index mask, and testing the hash index to identify the corresponding entry in the compressed state table located using the base address pointer, the following testing step against the test value and the following steps being performed on the maximum of N state-transition rules of the identified compressed state table entry.

3. (currently amended) The method of claim 1 ~~or 2~~, further comprising the step of :

- dividing the compressed state table into more than one compressed state subtable; and,

- extending in each of the compressed state subtables, each state-transition rule with a corresponding index mask and a base address pointer of the compressed state subtable of the next state in said state-transition rule;

said method being also characterized in that it further comprises the step of initializing a current compressed state subtable base address pointer,

said method being finally also characterized in that the base address pointer of a matching entry becomes the current base address pointer of the compressed state of the next state.

4. (currently amended) An apparatus for deep packet processing comprising means adapted for implementing the steps of the method according to ~~anyone of claims 1 to 3~~ claim 1.

5. (currently amended) A chip embedded apparatus comprising means adapted for implementing the steps of the method according to ~~anyone of claims 1 to 3~~ claim 1.

6. (currently amended) A computer program product comprising programming code instructions for executing the steps of the method according to ~~anyone of claims 1 to 3~~ claim 1 when said program is executed on a computer.

~~7~~. (new) The method of claim 2, further comprising the step of :

- dividing the compressed state table into more than one compressed state subtable; and,

- extending in each of the compressed state subtables, each state-transition rule with a corresponding index mask and a base address pointer of the compressed state subtable of the next state in said state-transition rule;

said method being also characterized in that it further comprises the step of initializing a current compressed state subtable base address pointer,

said method being finally also characterized in that the base address pointer of a matching entry becomes the current base address pointer of the compressed state of the next state.

8. (new) An apparatus for deep packet processing comprising means adapted for implementing the steps of the method according to claim 2.

9. (new) A chip embedded apparatus comprising means adapted for implementing the steps of the method according to claim 2.

10. (new) A computer program product comprising programming code instructions for executing the steps of the method according to claim 2 when said program is executed on a computer.

11. (new) An apparatus for deep packet processing comprising means adapted for implementing the steps of the method according to claim 3.

12. (new) A chip embedded apparatus comprising means adapted for implementing the steps of the method according to claim 3.

13. (new) A computer program product comprising programming code instructions for executing the steps of the method according to claim 3 when said program is executed on a computer.

14. (new) An apparatus to perform deep packet processing on an input variable word bit chain, said apparatus comprising:

- means for creating a state table based on at least one initial state, and a final state, each state table entry defining a state-transition rule comprising a s-bit current state, a n-bit word of the input variable word bit chain and as-bit next state;

- means for converting the entries of the state table into a reduced number of state-transition rule entries, each entry containing a ternary match condition expressed as a s+n-bit test value and a s+n-bit test mask to be applied to the current state and the input word in combination, said each entry further containing the s-bit next state;

- means for ordering the reduced state table entries obtained by the execution of the preceding step, in a prioritized order, with most frequently used state-transition rules having the highest priority;

- means for initializing a current state as being the initial state and the first word of the chain being a current input word;

- means for testing the current state and the current input in combination, against the test value, using the test mask, in all the entries of the reduced state table until a match is found on at least one entry;

- means for selecting one entry with the highest priority, if multiple entries match;

- means for defining the next word of the input word chain as being the current input and the next state being the current state, if the next state read in the state-transition rule of a selected matching entry is not a final state; and,

- means for repetitively employing the means for testing, the means for selecting, and the means for defining until a final state is found.

15. (new) The apparatus of claim 14, further comprising:

- means for dividing the compressed state table into more than one compressed state subtable; and,

- means for extending in each of the compressed state subtables, each state-transition rule with a corresponding index mask and a base address pointer of the compressed state subtable of the next state in said state-transition rule;

said apparatus being also characterized in that it further comprises means for initializing a current compressed state subtable base address pointer,

said apparatus being finally also characterized in that the base address pointer of a matching entry becomes the current base address pointer of the compressed state of the next state.

20 ~~16~~. (new) A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing deep packet processing, the computer readable program code means in said computer program product comprising computer readable program code means for causing a computer to effect the functions of claim 14.

21 ~~17~~. (new) A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing deep packet processing, the computer readable program code means in said computer program product comprising computer readable program code means for causing a computer to effect the functions of claim 15.

22 ~~18~~. (new) An article of manufacture comprising a computer usable medium having computer readable program code means embodied therein for causing deep packet processing, the computer readable program code means in said article of manufacture comprising computer readable program code means for causing a computer to effect the steps of claim 1.

23 ~~19~~. (new) An article of manufacture comprising a computer usable medium having computer readable program code means embodied therein for causing deep packet processing, the computer readable program code means in said article of manufacture comprising computer readable program code means for causing a computer to effect the steps of claim 2.

20. (new) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for deep packet processing, said method steps comprising the steps of claim 1.